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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : G06F 9/445 — A1

(11) International Publication Number: **WO 00/41073**

(43) International Publication Date: 13 July 2000 (13.07.00)

(21) International Application Number: PCT/SE00/00005

(22) International Filing Date: 3 January 2000 (03.01.00)

(30) Priority Data:
09/226,166 7 January 1999 (07.01.99) US

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(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: PLUG AND PLAY I²C SLAVE

(57) Abstract

In accordance with embodiments of the invention, an electronic device including one or more controllers and one or more slave units is provided with a bus such as an I²C serial bus that connects the controllers and the slave units. The device further includes a secondary memory containing software drivers for a variety of different types of slave units, which can be present on the bus. The controller determines which types of slave units are actually present on the bus by sending, for each type of slave unit represented by a corresponding software driver in the secondary memory, a command via the bus using an address for the type. After determining which types of slave units are present on the bus, the controller loads correponding software drivers from the secondary memory into a RAM, and using the loaded software drivers to initialize the slave units present on the bus.

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PLUG AND PLAY I2C SLAVE

FIELD OF THE INVENTION

The present invention relates generally to data communications within a device or system, and in particular to data communications to and from removable components within the device or system via a serial bus.

BACKGROUND OF THE INVENTION

Conventional solutions for implementing data communications within electronic devices and systems, where at least some of the components are removable and exchangeable, are aimed at special products and are not general and easy to adapt to other systems. These conventional solutions often require that specialized hardware be added to standard system configurations to support interchangeability of different components. The additional, specialized hardware can include, for example, an additional bus that is used for identifying modules connected to the system, and non-standard, specially designed modules. These features typically increase both production costs and device complexity.

U.K. Patent Application No. 2 195 028 A, published March 23, 1988, discloses an apparatus for testing electrical circuits that includes a controller to which selected interface modules can be connected, to enhance functionality of the apparatus. The controller can interrogate the connected modules to determine both the physical location of each module within the apparatus, and function and character of each module. With this information the controller can appropriately organize its internal routines. However, the disclosed bus structure of the apparatus has a multiplicity of specialized buses including a parallel module

identification bus. Furthermore, the necessary size of the module identification bus varies depending on the number of modules that can be connected to the apparatus.

U.S. Patent No. 5,339,362 to Harris discloses an automotive audio system having a controller housing into which modular signal processing components can be inserted. A controller in the audio system polls all positions within the controller housing to determine which components are installed, and then configures itself via software to provide appropriate control functions. In the polling process the controller uses an 8-line wide SELECT bus as well as a specific POLL line. Furthermore, the patent disclosure suggests that all software routines for modular components that can be inserted into the system are stored in RAM, regardless of whether the corresponding modular components are actually inserted in the system.

Thus, the conventional solutions demonstrated in U.K. Patent Application No. 2 195 028 A and U.S. Patent No. 5,339,362 require large and/or multiple parallel buses, non-standard configurations and protocols, and large RAM capacity.

SUMMARY OF THE INVENTION

In accordance with embodiments of the invention, an electronic device including one or more controllers and one or more slave units is provided with an I^2C serial bus connecting the controllers and the slave units. The device further includes a secondary memory containing software drivers for a variety of different types of slave units.

The controller determines which types of slave units are present on the bus by sending, for each type of slave unit represented by a corresponding software driver in the secondary memory, a command via the bus using an address for the type. If the controller subsequently receives an acknowledge signal corresponding to the command, then the controller knows that a slave unit of the type indicated by the address is present on the bus. The controller continues sending commands

using different addresses, until either a predetermined number of slave units have acknowledged, or until commands corresponding to all of the slave unit types represented by software drivers stored in the secondary memory have been sent.

A corresponding software driver for each slave unit type present on the bus is loaded from the secondary memory into a RAM easily accessed by the controller. The software drivers can be loaded as they are identified, or can be loaded after all slave unit types present on the bus have been determined. The software drivers are used to initialize the slave units present on the bus and to enable the controller to properly coordinate and implement the device functions. Other serial buses and/or bus standards that support individual addressing and acknowledging can be used instead of the I^2C bus.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent to those skilled in the art from the following detailed description of preferred embodiments, when read in conjunction with the accompanying drawings. Like elements in the drawings have been designated by like reference numerals.

FIG. 1 shows exemplary connections in a device using an I^2C bus.

FIG. 2 shows an I^2C communication protocol.

FIG. 3 shows an I^2C communication protocol with a repeated start condition.

FIG. 4 shows an I^2C serial bus timing.

FIG. 5 shows an acknowledgment mechanism in accordance with the I^2C protocol.

FIG. 6 shows an acknowledgment mechanism outlined in an I^2C timing diagram.

FIG. 7A shows a device configuration in accordance with an embodiment of the invention.

FIG. 7B shows a device configuration in accordance with another embodiment of the invention.

FIG. 8 shows a flowchart of a device identification procedure in accordance with an embodiment of the invention.

FIG. 9 shows a detailed flowchart of a device identification procedure in accordance with an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

In accordance with embodiments of the invention, a standard I^2C bus is used to within an electronic device having modular components such as removable slave units, to dynamically determine which slave units are connected to the bus. Software drivers corresponding to those slave units connected to the bus are loaded from a secondary memory into a RAM. Thus, the electronic device can be dynamically configured using a standard bus such as the I^2C bus, and using off-the-shelf modular components that are I^2C compatible. This allows consumption of RAM to be minimized, as well as reducing production costs by using standard, off-the-shelf technology without additional, specialized hardware. The invention also confers the significant advantage of allowing a manufacturer of a device that incorporates modular components connected by a standard I^2C bus, to substitute different modular components during manufacturing without having to alter the device design in any way. This can be particularly useful, for example, because it allows the manufacturer to equip the device with modular components from different vendors depending on component pricing, availability, etc., thus resulting in further reductions in manufacturing costs and in greater flexibility.

The I^2C protocol can be used for communicating data within a system having at least one microcomputer and other peripheral devices, e.g., memories and I/O expanders. The I^2C protocol is especially useful when the cost

of connecting various devices within the system must be minimized, and high speed data transfer is not required.

In particular, the I^2C protocol is a two-pin, bidirectional serial protocol that uses a data signal on one pin and a clock signal on the other pin. The protocol is symmetrical with respect to each of the pins, so that the same rules apply to bidirectional transfer of data information through the data pin as apply to bidirectional transfer of clock information through the clock pin. For a more thorough description of the I^2C protocol, see, e.g., *The I^2C-Bus and How to Use It (Including Specifications)*, Philips Semiconductors, copyright April 1995, pages 1-24, which is hereby incorporated by reference.

As shown in FIGS. 5 and 6, an Acknowledge signal put onto the bus by a slave unit in response to a command on the bus including an address for the slave unit, can be used to indicate that the slave unit is present on the bus. A system incorporating exemplary embodiments of the invention must be aware of which devices or slave units can be accepted within the system. This can be done, for example, directly in the software code provided for the controller within the system. Alternatively, the controller can be provided with a configuration file that will be evaluated when the software code for the controller is run, for example when the system is powered up. As outlined in the Philips specification for the I^2C standard, the I^2C standard requires that each slave on the bus respond to a unique address, and indicates that an I^2C-bus Committee coordinates allocation of unique I^2C addresses. In accordance with different embodiments of the invention, slave units present on an I^2C bus must be recognized or identified, and then initialized and/or operated using appropriate software drivers.

As shown in FIG. 7, in accordance with an embodiment of the invention incorporated within an electronic device, software drivers for all I^2C slave units that can be used within the device (in accordance with the particular function and application of the device) are stored in a secondary memory 710. The secondary

memory 710 can be, for example, an SRAM, an EEPROM, or any other suitable memory that can, for example, maintain its contents without an external power source. As shown in FIG. 7A, an exemplary device incorporating an embodiment of the invention includes a controller or microcontroller 706 and a slave unit such as an LCD driver 708. Alternatively, as shown in FIG. 7B, the secondary memory can be provided within the microcontroller 706, as secondary memory 714, or can be provided external to, but directly connected to, the microcontroller 706, as secondary memory 712.

FIG. 8 shows a flowchart describing the general function of an embodiment of the invention. After starting at step 810, in step 820 all slave units present on the bus are detected. This step can be performed, for example, by the microcontroller 706. In step 840, software drivers corresponding to all of the slave units determined to be present on the bus are loaded, for example into a RAM located within the microcontroller 706 or directly connected to the microcontroller 706. In step 850, the loaded software drivers are used to initialize the slave units present on the bus. After the slave units are initialized, the device incorporating the bus and the slave units proceeds with its characteristic functions.

FIG. 9 shows a flowchart showing an exemplary function of an embodiment of the invention in greater detail. After beginning in step 910, a counter is initialized in step 920, and then in step 930 an address from a list of addresses corresponding to slave unit types that can be present on the bus is obtained.

In step 940, a command is sent onto the bus using the address obtained in step 930. The command can be a dummy command, a power up command, or any other command that will elicit an acknowledge signal from any slave unit present on the bus that is of the type indicated or represented by the address. If an acknowledge is received, then in step 960 the slave unit type is added to a list that indicates types of slave units that are present on the bus.

In step 970, after the command has been sent and after, for example, either a predetermined period of time has elapsed or an acknowledge signal has been received, the counter is incremented in step 970 and then tested in step 980 to determine whether a predetermined number of different addresses have been used to send commands with. The predetermined number can be, for example, a number of slave unit types that must be present on the bus in order for the device incorporating the bus and the slave units to properly function. Alternatively, the predetermined number can be, for example, the total number of different slave unit types represented by corresponding software drivers that are stored in the secondary memory.

If in step 980 the counter equals the predetermined number, then in step 990 software drivers corresponding to the slave units present on the bus are loaded and used to initialize the slave units, and thereafter the device incorporating the bus and the slave units begins other functions in accordance with its intended purpose. If in step 980 the counter is less than the predetermined number, then control returns to step 930, and the cycle described above repeats.

Various alternatives can be employed in keeping with the spirit of the invention. For example, software drivers can be loaded and slave units can be initialized as each new slave unit type present on the bus is detected. Furthermore, in accordance with the I^2C specification, various controllers or other "master" devices can be included within the device and connected to the bus, and can work together or separately to determine the character of slave units or other units connected to the bus that require software drivers and/or initialization, and perform necessary initialization procedures and subsequently issue appropriate commands to the units connected to the bus. Furthermore, the detection and initialization cycle can be run as part of a power up sequence for the device, and/or can be periodically performed while the device is powered up so that "hot changeovers", *i.e.*, slave unit removals and additions performed while the device

is powered up, can be detected and compensated for. In accordance with principles of the invention, various embodiments of the present invention can employ serial buses other than the I^2C bus, which support individual addressing and acknowledging. Such buses can include, for example, support for a command that will elicit detailed identification information from a slave unit on the bus. In accordance with various embodiments of the invention, the contents of the secondary memory can also be updated.

It will be appreciated by those skilled in the art that the present invention can be embodied in other specific forms without departing from the spirit or essential characteristics thereof, and that the invention is not limited to the specific embodiments described herein. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims rather than the foregoing description, and all changes that come within the meaning and range and equivalents thereof are intended to be embraced therein.

Claims:

1. A electronic device, comprising:

at least one controller;

at least one slave unit;

a bus connecting the at least one controller and the at least one slave unit and functioning in accordance with a protocol that supports individual addressing and acknowledging; and

a secondary memory containing software drivers for a plurality of different types of slave units; wherein

the at least one controller initializes each at least one slave unit by sending a query over the bus for each type of slave unit in a predetermined group of types of slave units, retrieving a corresponding software driver for each at least one slave unit that responds to the query, and performing initialization operations using the software driver; and

the at least one controller and the at least one slave unit are connected only by the serial bus.

2. The device of claim 1, wherein the bus is an I^2C bus.

3. The device of claim 1, wherein the secondary memory is an EEPROM.

4. The device of claim 1, wherein the secondary memory is a static RAM.

5. The device of claim 1, wherein the secondary memory is connected to the bus.

6. The device of claim 1, wherein the secondary memory is directly connected to the at least one controller.

7. The device of claim 1, wherein the query is a power down command.

8. The device of claim 1, wherein the query is a dummy command.

9. The device of claim 1, wherein the bus consists of two lines.

10. The device of claim 1, wherein the bus is a serial bus.

11. A method for configuring an electronic device including at least one controller, at least one slave unit, a bus connecting the at least one controller and the at least one slave unit, and a secondary memory containing software drivers for a plurality of different types of slave units, comprising the steps of:

sending a command via the bus using an address for a type of slave unit;

receiving an acknowledge signal from a slave unit on the bus when the slave unit is of the type indicated by the address;

repeating the steps of sending and receiving using an address for a different type of slave unit until a predetermined number of acknowledge signals have been received;

loading a software driver from the secondary memory for each type of slave unit from which an acknowledge signal was received into a random access memory in the at least one controller; and

initializing each slave unit on the bus using the loaded software drivers.

12. The method of claim 11, further comprising the step of repeating the steps of sending and receiving using an address for a different type of slave unit until all addresses corresponding to the slave unit types of the software drivers in the secondary memory have been used.

13. The method of claim 11, wherein the steps of sending, receiving, loading and initializing are performed periodically while the electronic device is powered up.

14. The method of claim 13, further comprising the step of purging all software drivers from the random access memory of the at least one controller that correspond to slave unit types that are no longer present on the bus.

15. The method of claim 11, wherein the serial bus consists of two lines.

16. The method of claim 11, wherein the serial bus is an I^2C bus.

17. The method of claim 11, wherein the command is a dummy command.

18. The method of claim 11, wherein the command is a power up command.

19. The method of claim 11, wherein the command includes an instruction requiring a slave unit that is present on the bus and whose type corresponds to the address used to send the command, to provide information that further identifies the slave unit.

20. The method of claim 11, wherein the at least one controller maintains a configuration file identifying the slave units on the bus.

21. The method of claim 11, wherein the command requires a slave unit that is present on the bus and whose type corresponds to the address used to send the command, to send an acknowledge signal via the bus.

22. The method of claim 11, wherein the bus is a serial bus.

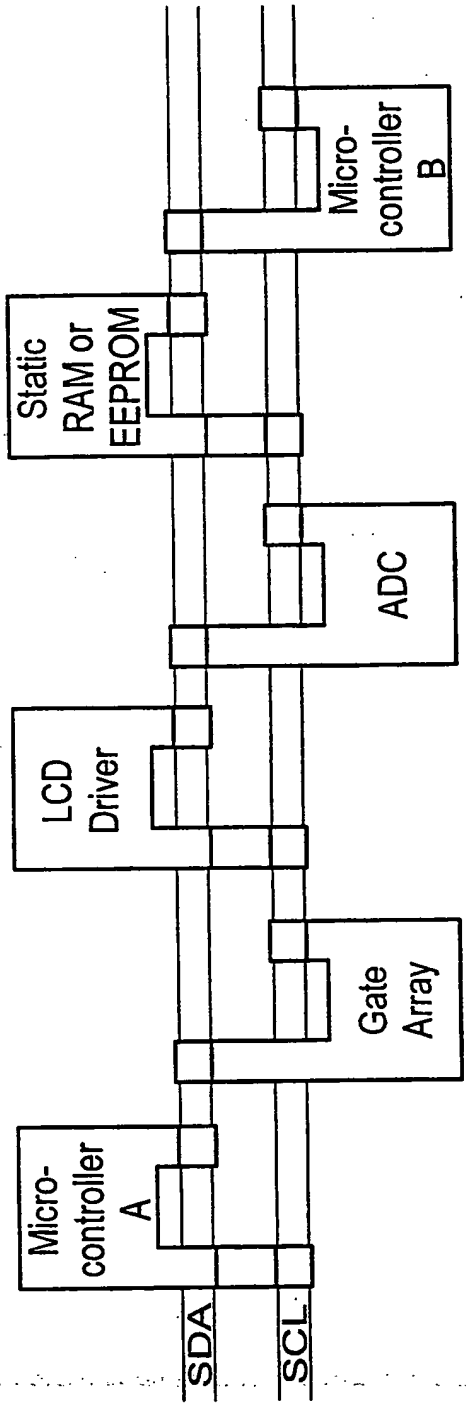


FIG. 1
(PRIOR ART)

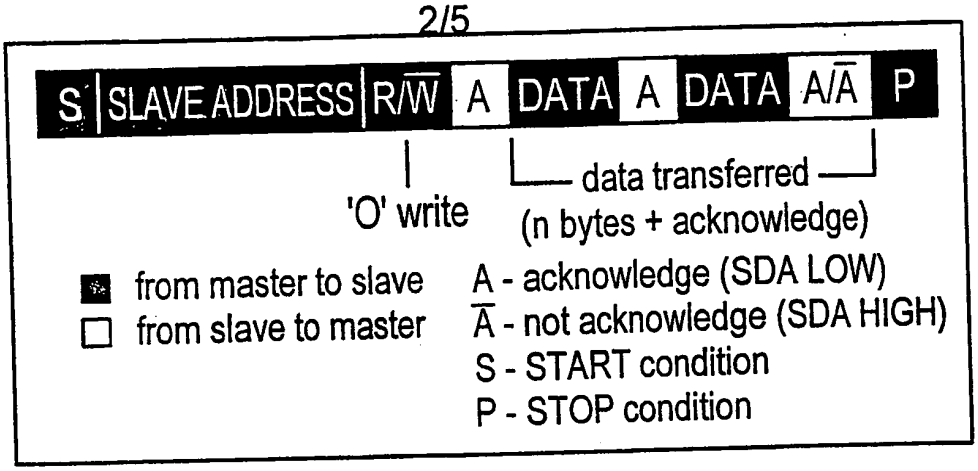


FIG. 2 (PRIOR ART)
I^2C communication protocol

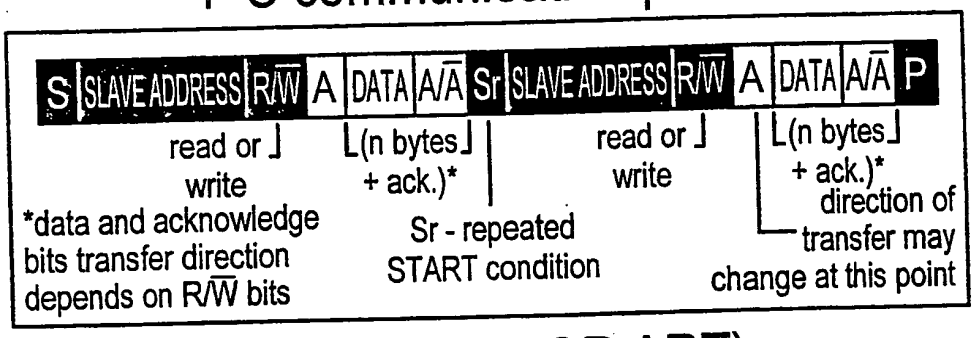


FIG. 3 (PRIOR ART)
I^2C communication protocol with a repeated start condition

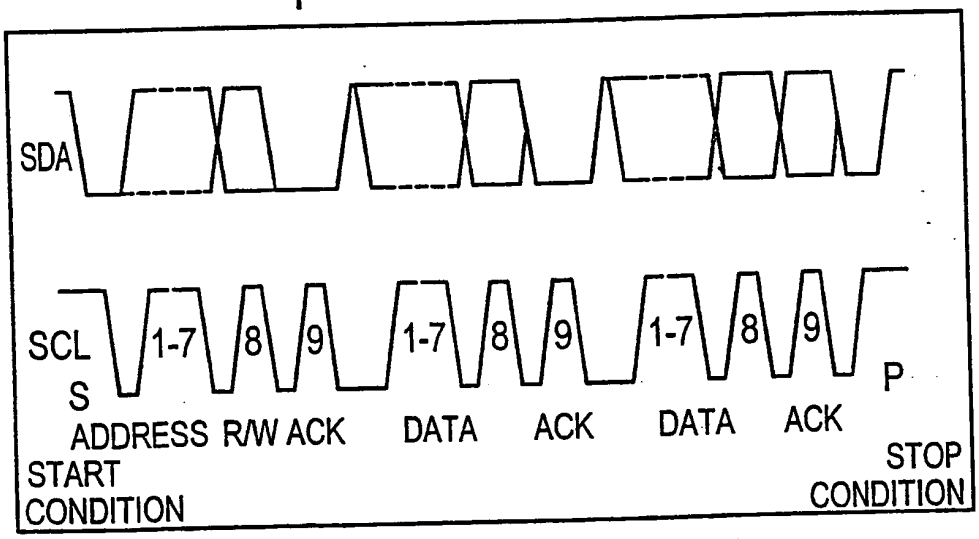


FIG. 4 (PRIOR ART)
I^2C serial bus timing

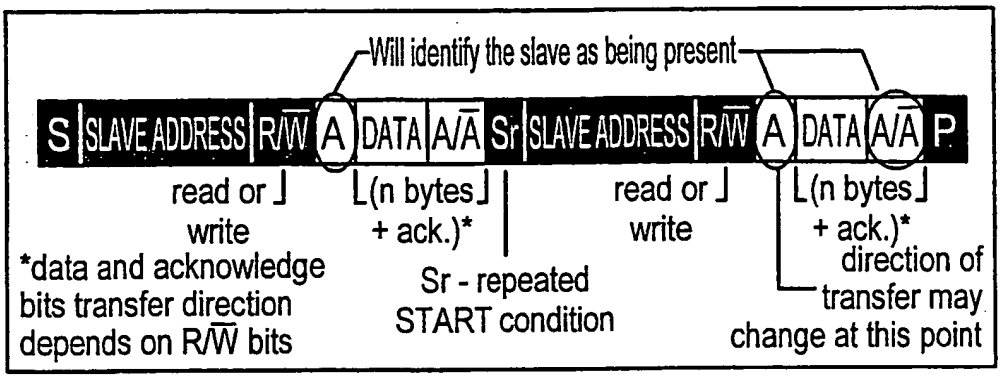


FIG. 5
Acknowledgement mechanism in the I^2C protocol

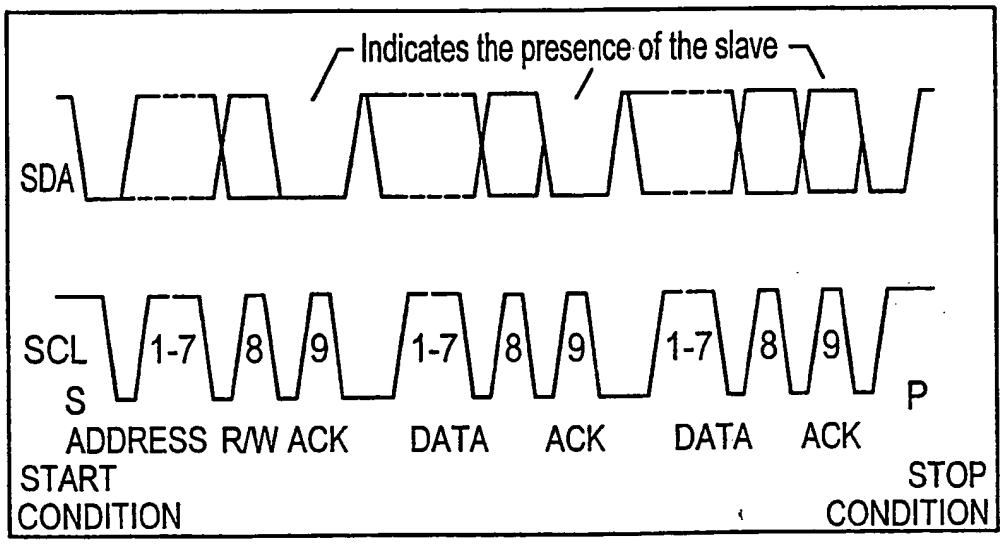


FIG. 6
Acknowledgement mechanism outlined in the I^2C timing diagram

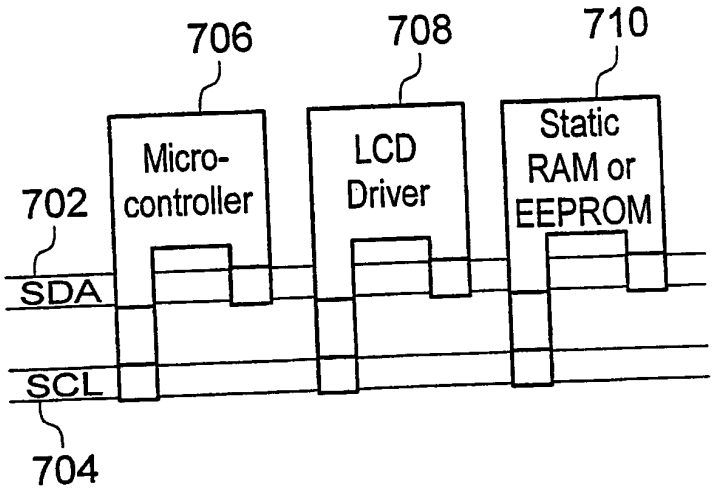
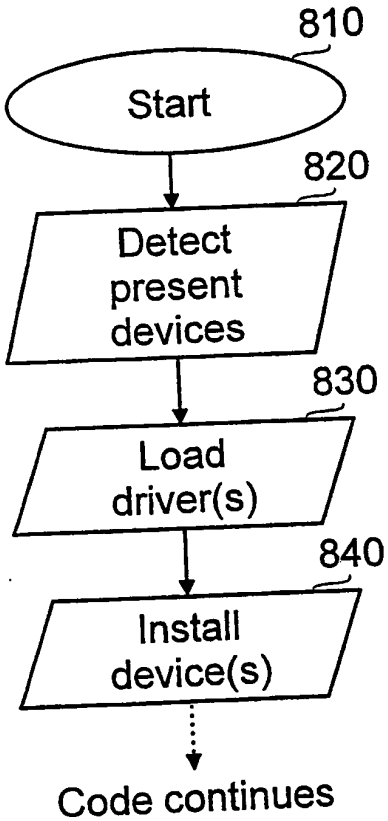


FIG. 7A



Top-level flowchart of the device identification procedure

FIG. 8

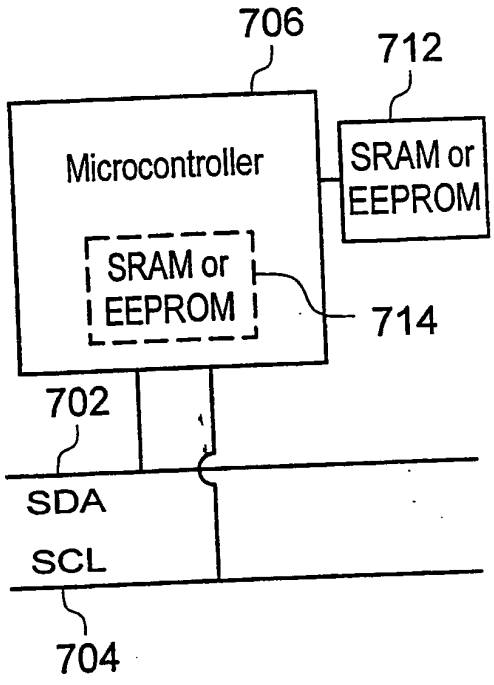


FIG. 7B

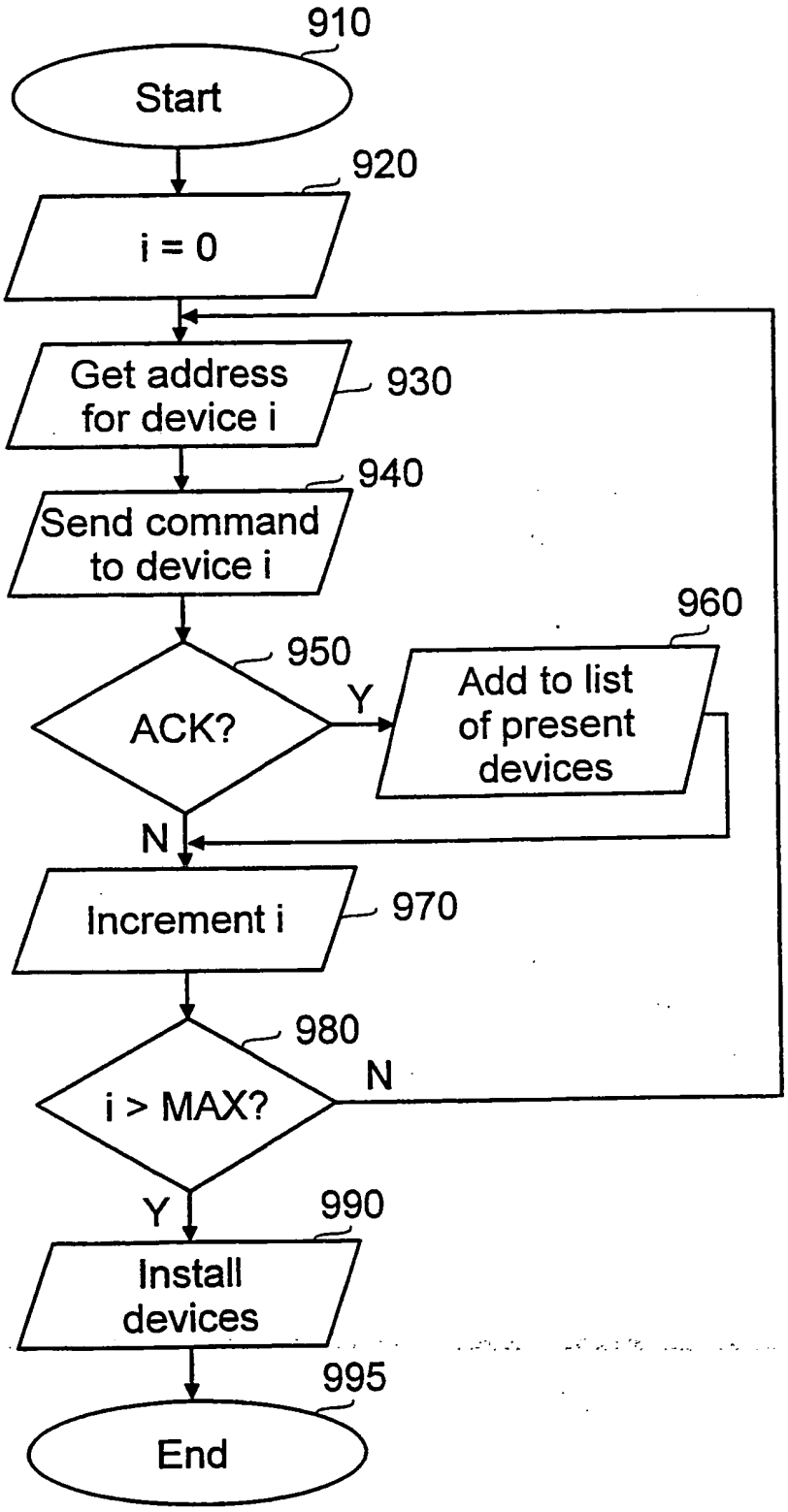

910
Start
920
i = 0
Get address for device i
930
940
Send command to device i
960
950
ACK?
Y
Add to list of present devices
N
Increment i
970
980
i > MAX?
N
Y
990
Install devices
995
End

FIG. 9

INTERNATIONAL SEARCH REPORT

Intern ıal Application No
PCT/SE 00/00005

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F9/445

According to International Patent Classification (IPC) or to both national classification and IPC

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Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5 794 032 A (LEYDA) 11 August 1998 (1998-08-11) column 5, line 36 -column 10, line 35; figures 1,3,4	1-11, 15-22 12
Y	US 5 668 992 A (HAMMER ET AL) 16 September 1997 (1997-09-16) abstract column 3, line 54 -column 4, line 4	12
A	"Unconditional Installation of SCSI Device Drivers" IBM TECHNICAL DISCLOSURE BULLETIN., vol. 37, no. 4A, April 1994 (1994-04), pages 153-154, XP000446222 NEW YORK US the whole document	1,11

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
17 April 2000	27/04/2000

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Intern ial Application No
PCT/SE 00/00005

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 325 532 A (CROWSSY ET AL) 28 June 1994 (1994-06-28) abstract	3,5

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

...formation on patent family members

Inter ...al Application No
PCT/SE 00/00005

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5794032 A	11-08-1998	US 5867730 A	02-02-1999
US 5668992 A	16-09-1997	BR 9502940 A	21-05-1996
		CA 2150742 A	02-02-1996
		CN 1128373 A	07-08-1996
		CZ 9700253 A	17-12-1997
		DE 69503056 D	23-07-1998
		DE 69503056 T	18-02-1999
		EP 0774136 A	21-05-1997
		WO 9604603 A	15-02-1996
		HU 77153 A	02-03-1998
		JP 8055018 A	27-02-1996
		PL 318373 A	09-06-1997
US 5325532 A	28-06-1994	AU 5138393 A	26-04-1994
		WO 9408288 A	14-04-1994